REMARKS

Examiner A. Roman is thanked for a complete search and thorough Office Action.

2. Reconsideration of the objections to the Abstract is respectfully requested for the following reasons.

The Abstract is amended to reduce the number of words. A clean copy of the amended Abstract is enclosed.

3. Reconsideration of the objections to the specification is respectfully requested for the following reasons.

On page 9 the term "The self-aligned" is replaced with --Self-aligned-- as requested by the Examiner, and is shown in the marked-up copy in the Appendix. Also, the end of the sentence in which the above change was made, ended with a semicolon (";") which is replaced with --.-- (a period).

4. Reconsideration of the objections to claim 21 is respectfully requested for the following reasons.

Claim 21, lines 1 and 24, the word "transistors" was replaced with --transistor-- and the phrase --doped with a-- was inserted in line 8 between the words "layer" and "second." A semicolon --;-- was inserted after the word "spacers" on line 18. These changes are shown in the marked-up copy of claim 21 in the Appendix.

7. Reconsideration of the rejection of claims 21 and 23-25 under 35 U.S.C. 102(e) as being anticipated by Cheek et al., U. S. Patent 6,018,180, is respectfully requested for the following reasons.

The structure in the prior art of Cheek et al. cited by the Examiner is significantly different from the applicant's structure.

There are three major differences between the prior-art structure of Cheek et al. and the applicant's structure.

1. Cheek et al. form a diffused region 380 by implanting (see col. 7, lines 19-31) using a photoresist mask 370 (see Fig. 5) prior to depositing an insulating layer 440 and etching a contact opening 450. Therefore, the void 460 (Fig. 10) is etched into the field oxide 220 and can be etched below (over-etched) the diffused region 380, causing shorts.

The applicant's implant is performed (see Fig. 4) after etching the opening 2, as shown in Fig. 3, and is therefore implanted in the over-etched region X, as shown in Fig. 4. Therefore, the implant region G is conformal to the over-etched region X, and is independent of how deep the over-etched region of the STI is.

2. As pointed out above Cheek et al. use a separate photoresist mask 370 (col. 6, lines 15-34) to ion implant the region 380 (col. 7, lines 29-31) before depositing the insulating layer 440 (col. 7, lines 44-49) in which trenches L1 (contact openings) 450 are etched (col. 7, lines 49-51).

Therefore, Cheek's diffusion 380 cannot be self-aligned to the opening 450.

The applicant's implanted region G (see Fig. 4) is done after the opening 2 is etched, and therefore the implanted region G is self-aligned to the opening 2 and is also self-aligned to the over-etched region X in the STI 12.

3. Cheek et al. must form the diffused region 380 deeper than the source/drain region 320 to effectively prevent shorts when the void 460 is etched in the STI oxide 220 below the junction 340 of the source/drain region 320.

The applicant does not need to implant below the source/drain area 19' to prevent shorts. Therefore, the source/drain areas can remain shallow, as required for advanced high-performance circuits.

The applicant's relatively low-energy implant in the region X at the STI-source/drain interface effectively forms a diffused region G conformal to the region X that prevents shorts, as shown in Fig. 4.

The applicant's structure is not anticipated by Cheek et al. and therefore is patentable over Cheek et al.

Claims 23-25 are dependent claims that do not stand on their own merits but support the independent claim 21.

10. Reconsideration of the rejection of claim 22 under 35 U.S.C. 103(a) as being unpatentable over Cheek et al. is respectfully requested for the following reasons.

Claim 22 is a dependent claim that does not stand on its own merits but supports the independent claim 21.

11. The prior-art references made of record but not relied upon were reviewed and were found not to negate the applicant's invention. In Okada et al. Fig. 19d, the diffused region 13 is formed by implanting below the source/drain area 8, and therefore Okada's invention is not similar to the applicant's structure. In Furuta et al. the source/drain regions 9 are formed by implanting through a conductive film 8, such as polysilicon or polycide, and therefore is not similar to the applicant's invention. Kuroda utilizes a silicon film that is patterned over the source/drain areas to protect the field oxide 12/silicon substrate 11 interface from over-etching, as shown in the sequence of process steps in Figs. 1A-1E. Kim teaches a method for making concurrently a contact to an N-channel and a P-channel FET by deliberately etching a field oxide in a trench between the two FETs, and using two masking steps to dope the sidewalls in the trench P^+ for the P-channel FET, and N^+ for the N-channel FET. This is not the applicant's structure. Ha et al. teach a method for making a contact over the interface between an insulating layer 120 and a substrate 100 having a doped surface 140. In Ha's embodiments the implant in the contact openings is deeper than the diffused area 140 (as shown in Figs. 4C, 5C, and

6C), and therefore Ha et al. would not achieve the applicant's structure.

It is requested that Examiner A. Roman call the undersigned Attorney at (845) 452-5863 should there be anything that can be done to help bring this Patent Application to Allowance.

Respectfully submitted,

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PLEASE AMEND THE CLAIMS - MARKED-UP COPY

21. (AMENDED) A Salicide field effect transistor [transistors] with improved borderless contact [contacts] openings comprised of:

a semiconductor substrate doped with a first conductive type dopant and having device areas surrounded and electrically isolated shallow trench field oxide areas;

a gate oxide layer on said device areas, and a conductively doped patterned polysilicon layer doped with a second conductive type dopant over said device areas for gate electrodes;

lightly doped source/drain areas with said second conductive type dopant in said device areas adjacent to said gate electrodes and an insulating sidewall spacers on the sidewalls of said gate electrodes;

heavily doped first source/drain contact areas composed of said second conductive type dopant in said device areas adjacent to said insulating sidewall spacers;

a silicide layer on said gate electrodes and on said source/drain contact providing said Salicide field effect transistors;

a conformal barrier layer, and an interlevel dielectric layer on said Salicide field effect transistor [transistors];

borderless contact openings in said interlevel dielectric layer and said barrier layer to said source/drain areas and extending over said field oxide with unintentional over-etched field oxide regions at said field oxide-source/drain area interface;

a dopant composed of said second conductive type in said substrate under and adjacent to said over-etched field oxide regions in said borderless contact openings providing said source/drain contact areas with a continuous doped region around said over-etched field oxide regions.

PLEASE AMEND THE SPECIFICATION - PAGES 8-10

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The method consist of providing a semiconductor substrate doped with a first conductive type dopant. The substrate typically is single crystal silicon and is doped with P-type dopant, such as boron (B). A shallow trench isolation (STI) field oxide (FOX) areas is formed in and on the substrate and surrounds and electrically isolates device areas on the substrate. A thin gate oxide is formed on the device areas usually by growing a silicon oxide (SiO_2) layer by thermal oxidation. A conductively doped polysilicon layer is formed by depositing a polysilicon which is doped with an N-type conductive dopant. The N doped polysilicon

layer is patterned to include gate electrodes over device areas. Next lightly doped source/drain areas are formed in the device areas adjacent to said gate electrodes by ion implantation, using a second conductive type dopant (N-dopant), such as arsenic ions (As^{75}) or phosphorus (P^{31}). Insulating sidewall spacers are formed on the sidewalls of the gate electrodes by depositing a conformal silicon oxide layer by chemical vapor deposition (CVD) and anisotropically plasma etching back the CVD-SiO_2. During the etch back, the top surface of the polysilicon gate electrodes and the source/drain contact areas are exposed. Next, optional, heavily doped source/drain contact areas are formed in the device areas adjacent to the sidewall spacers by ion implanting a the second conductive type dopant, such as As or P. [The self-aligned] Self-aligned silicide (SALICIDE) FETs are formed next by depositing a relatively thin conformal metal layer, such as titanium (Ti) or cobalt (Co), on the substrate over the gate electrodes and the device areas[;]. A first thermal anneal, preferably a rapid thermal anneal (RTA-1) is carried out to selectively form a silicide layer ($TiSi_x$ or a CoSix) on the top surface of the gate electrodes and on the source/ drain contact areas. The unreacted metal layer on the oxide sidewall spacer and other oxide surfaces (e.g. STI) is then removed by selectively wet etching. Next, a conformal etch stop/barrier layer, composed of Si_3N_4 or silicon oxynitride (SiON), is deposited by CVD. An interlevel dielectric (ILD) layer, for example

composed of CVD-SiO_2 is deposited over the etch stop layer and provides electrical insulation for the next level of electrical interconnection. The ILD layer is typically planarized. Next, borderless contact openings are etched in the ILD layer to the source/drain areas. These borderless contact openings extend over the field oxide. Typically, because of the nonuniformity of the ILD layer and the nonuniformity etch rate across the substrate it is necessary to over etch to insure that all contacts openings are open across the substrate. Unfortunately, this results in over etching the field oxide regions (STI) at the field oxide-source/drain area interface and results in source/drain-to-substrate shorts when conducting plugs, such as metal plugs, are subsequently formed in the contact openings. Now, by the method of this invention, a contact dopant is ion implanted in the substrate under and adjacent to the over-etched field oxide regions in the borderless contact openings. The second thermal anneal, preferably a second RTA (RTA-2), is performed to complete the phase transition of the metal silicide (to reduces sheet resistance) and concurrently to active the ion implanted contact dopant to form source/drain contact areas that are continuous around the over-etched field oxide regions. This modified diffused metallurgical junction reduces the electrical shorts when conducting plugs are later formed in the borderless contact openings. Since the contact implant is integrated into the salicide FET process the thermal

budget for the process is not increased, which is essential for future shallow junction devices.